

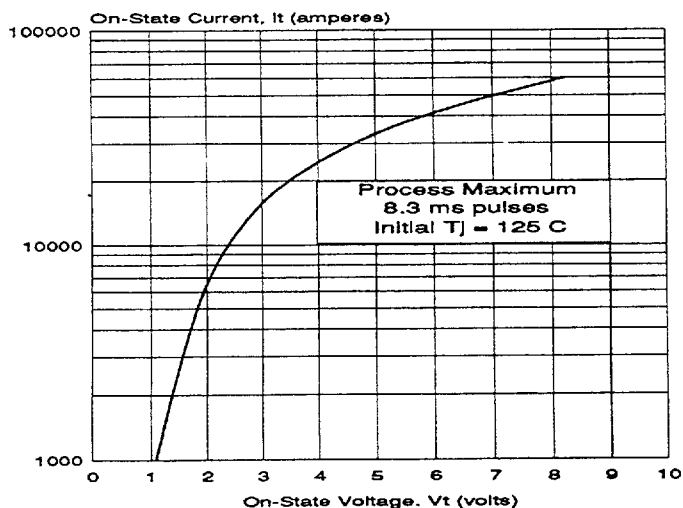
THYRISTOR XSDT306

100mm / 2000V / 4200A avg / 200us

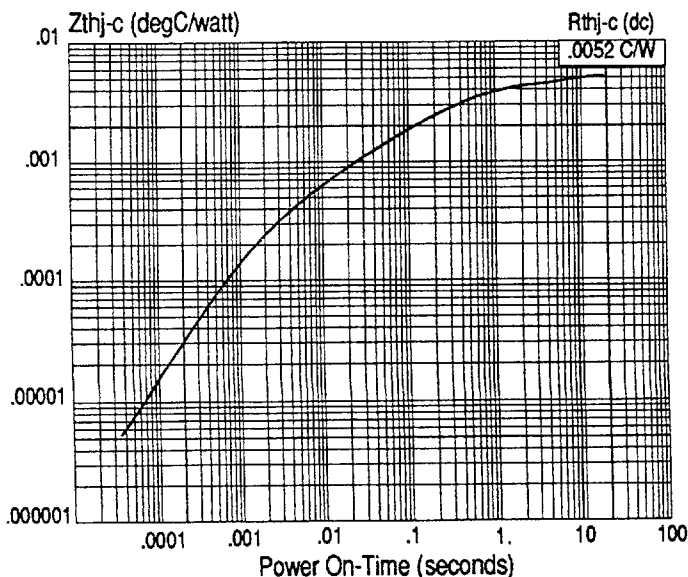
Type SDT306 reverse blocking thyristor is suitable for inverter applications. The silicon junction is manufactured by the proven multi-diffusion process and utilizes the exclusive involute gate structure. It is supplied in an industry accepted disc-type package, ready to mount using commercially available heat dissipators and mechanical clamping hardware.

Prefix "X" signifies that the product is in the final stage of design. Some characteristics may change in the final design.

ON-STATE CHARACTERISTIC



THERMAL IMPEDANCE junction to case (dc)



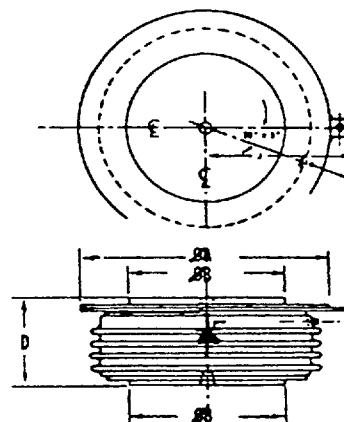
REPETITIVE BLOCKING VOLTAGE OFF-STATE AND REVERSE

MODEL	V_{DRM} / V_{RRM} 0 to +125°C	@ -40°C
XSDT306TT	2000 volts	1900 volts
XSDT306TS	1900	1800
XSDT306TR	1800	1700
XSDT306TP	1700	1600
XSDT306TM	1600	1500
XSDT306TK	1500	1400

Gate Drive Requirements:
30V / 10 ohms / 0.5us risetime
10 - 20 us minimum duration

External Clamping Force:
17000-19000 lbs.
75.6 - 84.5 kN

MECHANICAL OUTLINE



$\varnothing A = 5.6$ in (142 mm)
 $\varnothing B = 3.9$ in (99 mm)
 $D = 1.5$ in (38 mm)

**ELECTRICAL
CREEPAGE / STRIKE**

1.6 / 1.0 in
40.6 / 25.4 mm

**CLAMPING FORCE
(range)**
17000-19000 lb.

SILICON POWER CORPORATION
175 GREAT VALLEY PKWY. MALVERN, PA 19355
USA

94g: 7/13/95

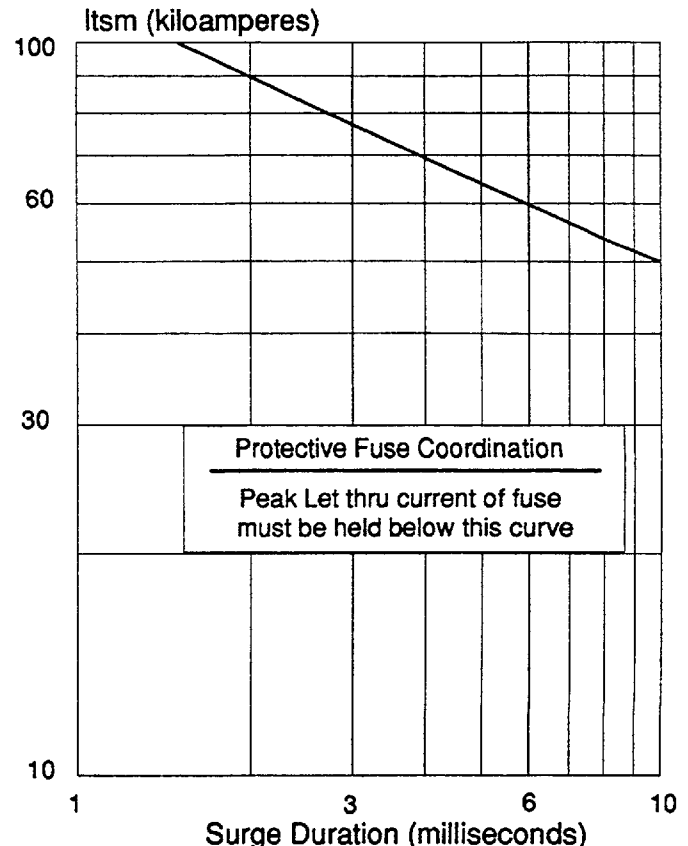
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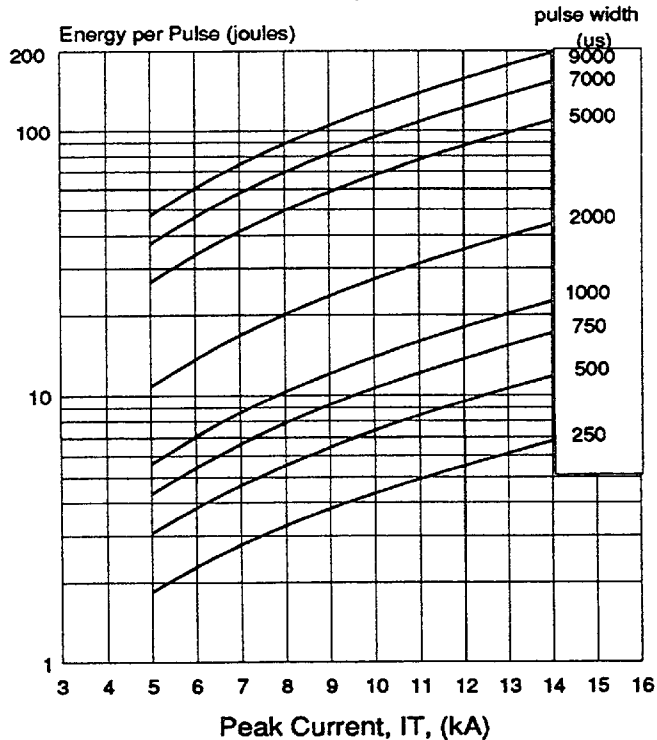
LIMITING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT	UNITS
Repetitive peak off-state & reverse voltage	V_{DRM}/V_{RRM}	$T_j = -40$ to $+125^\circ\text{C}$	up to 2000V	volts
Off-state & reverse current	I_{DM}/I_{RM}	$T_j = 125^\circ\text{C}$	—	ma
Peak half cycle non-repetitive surge current	I_{TSM}	60Hz (8.3ms) 50Hz (10ms)	53 50	(kA)
On-state voltage	V_{TM}	$I_T = 4000\text{A}$ $t_p = 8.3\text{ms}$ $T_j = 125^\circ\text{C}$	1.70	volts
Average on-state current	$I_{T(av)}$	$T_c = 70^\circ\text{C}$	4200	A
Critical rate of rise of on-state current	di/dt_{top}	$V_D = 60\% V_{DRM}$ 60Hz $T_j = 125^\circ\text{C}$ see gate drive	300	A/us
Critical rate of rise of off-state voltage	dv/dt	$V_{DCRIT} = 80\% V_{DRM}$ $T_j = 125^\circ\text{C}$	500	v/us
Peak recovery current	I_{RM}	$T_j = 125^\circ\text{C}$ @ 10A/us @ 50A/us @ 100 A/us	— — —	A
Circuit commutated turn-off time	t_Q	400V/us to 80% V_{DRM} $V_r = > 50\text{V}$	200	us

Maximum Non-Repetitive Surge Current
Peak Half-Sine Current



ON-STATE ENERGY
half-sine pulses



84g

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